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AMENDMENTS TO THE CLAIMS:

1. (Currently amended) A method of making an electronic interconnection, said method comprising:

for a signal line to be interconnected, using a plurality of bonding wires configured to provide a controlled impedance effect, wherein both a signal current and a return current are conducted by said plurality of bonding wires.

2. (Currently amended) The method of claim 1, wherein said plurality of bonding wires is configured such that a first bonding wire is located a predetermined distance above a second bonding wire to provide at least a part of said controlled impedance effect.

3. (Currently amended) The method of claim 1, wherein said plurality of bonding wires is configured such that a first bonding wire is located a predetermined distance alongside a second bonding wire to provide at least a part of said controlled impedance effect.

4. (Original) The method of claim 1, wherein one of a first bonding wire and a second bonding wire of said plurality of bonding wires is grounded.

5. (Currently amended) The method of claim 1, further comprising:

providing a dielectric material such that a predetermined distance is maintained by said dielectric material separating a first bonding wire and a second bonding wire of said plurality of bonding wires to provide at least a part of said controlled impedance effect.

6. (Original) The method of claim 5, wherein said dielectric material is periodically placed along a length of said plurality of bonding wires.

7. (Original) The method of claim 5, wherein said dielectric material is continuously placed along a length of said plurality of bonding wires.

8. (Original) The method of claim 5, wherein said dielectric material comprises an ultraviolet-cured epoxy.

9. (Original) The method of claim 3, wherein a third bonding wire is located a predetermined distance alongside said first bonding wire and said second bonding wire.

10. (Currently amended) The method of claim 1, further comprising:

substantially simultaneously co-dispensing bonding wires of said plurality of bonding.

11. (Currently amended) The method of claim 1, further comprising:

substantially simultaneously dispensing said bonding wires in said plurality of bonding wires so that said bonding wires are separated by predetermined distances;

substantially simultaneously co-dispensing a dielectric material with said bonding wires, said dielectric material thereby maintaining said predetermined distances of said bonding wires.

12. (Currently amended) The method of claim 1, wherein said bonding wires of said signal line comprise a plurality of round bonding wires.

13. (Currently amended) The method of claim 1, wherein said bonding wires of said signal line comprise a plurality of ribbon bonding wires.

14. (Currently amended) The method of claim 1, wherein said bonding wires of said signal line comprise a combination of at least one round bonding wire and at least one ribbon wire.

15. (Original) The method of claim 1, wherein said plurality of bonding wires for said signal comprises a microstrip.

16. (Original) The method of claim 1, wherein said plurality of bonding wires for said signal comprises a coplanar waveguide.

17. (Original) The method of claim 1, wherein said signal comprises a single-ended signal.

18. (Original) The method of claim 1, wherein said signal comprises a differential signal.

19. (Original) The method of claim 5, wherein said dielectric material includes particles having a high dielectric constant.

20. (Original) The method of claim 19, wherein said particles comprise at least one of glass and ceramic.

21. (Original) The method of claim 19, wherein a spacing of intervals of said particles permits an effect of one of a filter and an impedance transformer.

22. (Original) The method of claim 6, wherein a spacing of said dielectric material permits an effect of one of a filter and an impedance transformer.

23. (Currently amended) A method of reducing high frequency parasitic effects in a chip transition, said method comprising:

for a signal in said transition, using a plurality of bonding wires configured to provide a controlled impedance effect, wherein both a signal current and a return current are conducted by said plurality of bonding wires.

24. (Currently amended) A method of fabricating an electronic component, said method comprising:

for a device in said electronic component, using a plurality of bonding wires configured to provide a controlled impedance effect for a signal line connecting to said device, wherein both a signal current and a return current are conducted by said plurality of bonding wires.

25. (Currently amended - Withdrawn) An electronic component comprising:

at least one signal line interconnected such that a plurality of bonding wires is configured to provide a controlled impedance effect for said signal line, wherein both a signal current and a return current are conducted by said plurality of bonding wires.

26. (Original - Withdrawn) An electronic apparatus comprising:

at least one electronic component having at least one signal line interconnected in accordance with claim 25.

27. (Currently amended) A method of providing a signal from a chip, said method comprising:

for a signal of said chip, providing a controlled impedance signal line comprising a plurality of bonding wires configured to be separated by a predetermined distance, wherein both a signal current and a return current are conducted by said plurality of bonding wires.

28. (Original) The method of claim 27, wherein said controlled impedance is designed to be near in value to at least one of an impedance of a circuit of said chip and an impedance of a circuit to which said signal line is interconnecting said chip circuit.

29. (Original) The method of claim 28, wherein said predetermined distance is maintained by a dielectric material, said controlled impedance being determined by said predetermined distance and a dielectric constant of said dielectric material.

30. (Original) The method of claim 28, wherein said plurality of bonding wires are arranged in one of a microstrip configuration and a coplanar waveguide configuration.